## 8-1-9 Internal Circuits

## Pulse Inputs



Phase Z


## External Outputs



Note In the above figure, $A$ is active when sourcing outputs are set, and $B$ is active when sinking outputs are set.

## 8-2 Pulse I/O Board

## 8-2-1 Model

| Name | Model | Specifications |
| :---: | :--- | :--- |
| Pulse I/O Board | CQM1H-PLB21 | Two pulse input points and two <br> pulse output points |

## 8-2-2 Function

Pulse Inputs 1 and 2
The Pulse I/O Board is an Inner Board that supports two pulse inputs and two pulse outputs.
Pulse inputs 1 and 2 can be used as high-speed counters to count pulses input at either 50 kHz (signal phase) or 25 kHz (differential phase). Interrupt processing can be performed based on the present values (PV) of the counters.

## Input Mode

The following three Input Modes are available:

- Differential Phase Mode ( 4 x )


## Pulse Outputs 1 and 2

Ports 1 and 2

- Pulse/Direction Mode
- Up/Down Mode


## Interrupts

The Board can be set to execute an interrupt subroutine when the value of the high-speed counter matches a specified target value, or an interrupt subroutine when the PV falls within a specified comparison range.

Two 10 Hz to 50 kHz pulses can be output from port 1 and port 2. Both fixed and variable duty factors can be used.

- The fixed duty factor can raise or lower the frequency of the output from 10 Hz to 50 kHz smoothly.
- The variable duty factor enables pulse output to be performed using a duty factor ranging from $1 \%$ to $99 \%$.

Note While pulse inputs and pulse outputs can be performed simultaneously, it is not possible to use all high-speed counter and pulse output functionality at the same time. The Port Mode Setting (High-speed Counter Mode/Simple Positioning Mode) in the PC Setup (DM 6611) will determine which has full functionality enabled.

Two pulse inputs (high-speed counter) and two pulse outputs can be used simultaneously via ports 1 and 2 . To determine which has functional priority, the appropriate Port Mode setting must be entered in the PC Setup (DM 6611).

| Mode | Content | High-speed counter functions |  | Pulse output functions |  |  | DM 6611 setting |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Reading PV with PRV(62) | Highspeed counter interrupts with CTBL(63) | No trapezoidal acceleration/ deceleration (SPED(64)) | $\begin{aligned} & \text { Identical } \\ & \text { acceleration/ } \\ & \text { deceleration } \\ & \text { rates } \\ & \text { (PLS2(一)) } \end{aligned}$ | $\begin{aligned} & \text { Separate } \\ & \text { acceleration/ } \\ & \text { deceleration } \\ & \text { rates } \\ & \text { (ACC(一)) } \end{aligned}$ |  |
| Highspeed Counter Mode | High-speed counter given priority. <br> All high-speed counter functions are enabled. <br> Trapezoidal acceleration/ deceleration for pulse outputs is limited. | Yes | Yes | Yes |  | Mode 0 disabled (Modes 1 to 3 enabled) See note 1. | $\begin{aligned} & 0000 \\ & \mathrm{Hex} \end{aligned}$ |
| Simple Positioning Mode | Pulse output given priority. <br> All pulse output functions are enabled. <br> Interrupts for the high-speed counter are disabled. | Yes | No | Yes | Yes | Yes | $\begin{aligned} & 0001 \\ & \mathrm{Hex} \end{aligned}$ |

Note 1. Mode 0: Acceleration + Independent Mode; Mode 1: Acceleration + Continuous Mode; Mode 2: Deceleration + Independent Mode; Mode 3: Deceleration + Continuous Mode.
2. The port modes for both ports 1 and 2 is always set to the same mode, i.e., either High-speed Counter Mode and Simple Positioning Mode. The mode cannot be set separately for each port.

## 8-2-3 System Configuration



## 8-2-4 Applicable Inner Board Slot

The Pulse I/O Board can only be mounted in slot 2 (right slot) of the CQM1HCPU51/61 CPU Unit.


## 8-2-5 Names and Functions

The CQM1H-PLB21 Pulse I/O Board has a CN1 connector for pulse input 1 and pulse output 1, and a CN2 connector for pulse input 2 and pulse output 2.
CQM1H-PLB21 Pulse I/O Board


Compatible connector
Socket: XM2D-1501 (OMRON)
Hood: XM2S-1511 (OMRON)
Two Sockets and two Hoods are provided as standard with the Pulse I/O Board.

## LED Indicators



Lit when there is an error in the PC Setup settings for pulse I/O, or when operation is interrupted during pulse output.

## Pulse Output Indicators

| Indicator | Port | Function |
| :--- | :---: | :--- |
| CW1 | Port 1 | Lit during CW pulse output to port 1. |
|  |  | Lit during CCW pulse output to port 1. |
| CCW1 |  | Port 2 |
| CW2 | Lit during CW pulse output to port 2. |  |
|  |  | Lit during CCW pulse output to port 2. |

## Pulse Input Indicators

| Port 1 | Port 2 | Function |
| :--- | :--- | :--- |
| A1 | A2 | Lit when the phase-A pulse input is ON a the port. |
| B1 | B2 | Lit when the phase-B pulse input is ON at the port. |
| Z1 | Z2 | Lit when the phase-Z pulse input is ON at the port. |

## 8-2-6 CN1 and CN2 Pin Arrangement

The pin arrangements of connectors CN 1 and CN 2 are identical.

| Pin Arrangement | Pin No. | Name | Use |
| :---: | :---: | :---: | :---: |
|  | 1 | Common input | Pulse input |
|  | 2 | Pulse input Z: 24 V DC |  |
|  | 3 | Encoder input A: 24 V DC |  |
|  | 4 | Encoder input B: 24 V DC |  |
|  | 5 | CCW pulse output | Pulse output |
|  | 6 | CW pulse output/PWM(-) output |  |
|  | 7 | 5-V DC power supply for output |  |
|  | 8 | 5-V DC power supply for output |  |
|  | 9 | Pulse input Z: 12 V DC | Pulse input |
|  | 10 | Encoder input A: 12 V DC |  |
|  | 11 | Encoder input B: 12 V DC |  |
|  | 12 | Common output (0 V) | Pulse output |
|  | 13 | CCW pulse output (with 1.6-k |  |
|  | 14 | CW pulse output/PWM(-) output (with 1.6-k $\Omega$ resistance) |  |
|  | 15 | Power supply for output |  |
|  | Hood | Not used. | --- |

Note Refer to Appendix A Preparing Cables for Inner Boards for information about using a compatible connector (XM2D-1501 Socket with XM2S-1511 Hood) to construct a cable.

## 8-2-7 Wiring Examples

## Pulse Input Connections

Connect the encoder output to CN1 and CN2 as shown below according to the port Input Mode.

| CN1 pins | CN2 pins | Signal name | Encoder output |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Port 1 | Port 2 |  | Differential Phase Mode | Pulse/Direction Mode | Up/Down Mode |
| 3,10 | 3, 10 | Encoder input A | Encoder Phase A input | Directional signal input | Decrement pulse input |
| 4, 11 | 4, 11 | Encoder input B | Encoder Phase B input | Pulse input | Increment pulse input |



Note The function of encoder inputs A and B in Pulse/Direction Mode and Up/Down Mode differs from the High-speed Counter Board (CQM1H-CTB41).

## Wiring Example

The example below shows connections to an encoder with phases A, B, and Z.

(Do not share the power supply with other I/O.)


## Pulse Output Connections



1. Caution Do not supply both 5-V and 24-V DC power at the same time. Doing so will damage the internal circuits.

## Wiring Examples

The following examples show a Pulse I/O Board connected to a motor driver with a 5-V input.
Example 1: 5-V DC Power Supply


## Example 2: 24-V DC Power Supply


$\triangle$ Caution The 5-V DC or 24-V DC power supply for the outputs must be connected correctly.

## Pulse Output Connection Precautions

- Connect a 7 to 30 mA load to the pulse output. Use a bypass resistor if the load is smaller than 7 mA .
- The pulse output circuits on pins 13 and 14 have a built-in resistance of $1.6 \mathrm{k} \Omega$ ( $1 / 2 \mathrm{~W}$ ). Connect the pulse outputs as shown below according to the power supply and the motor driver specifications.

Open Collector Output


Output transistor

Output from Open Collector $1.6 \mathrm{k} \Omega$ Series Resistance
$\xrightarrow{\sim}$

The internal $1.6-\mathrm{k} \Omega(1 / 2 \mathrm{~W})$ resistance can be used as bypass resistance in the following way.
Example: $\mathbf{7 m A}$ output transistor current $=\mathbf{4 m A}$ load current $+\mathbf{~ m A}$ bypass current


- The transistors of the internal circuits of the pulse output section are OFF when pulse output is stopped.



## Example Configurations Using OMRON Servo Driver Cables



## 8-2-8 Specifications

| Item | Specifications |
| :---: | :---: |
| Name | Pulse I/O Board |
| Model number | CQM1H-PLB21 |
| Compatible CPU Units | CQM1H-CPU51/61 |
| Unit classification | CQM1H-series Inner Board |
| Mounting locations and number of Boards | One in Inner Board slot 2 (right slot) |
| Pulse inputs | 2 inputs (Refer to High-speed Counter Pulse Inputs below for details.) |
| Pulse outputs | 2 outputs (Refer to Pulse Outputs below for details.) |
| Setting section | None |
| Indicators | Front: 12 LEDs 1 each of Ready (RDY) and Error (ERR) <br> 2 each of phase $A(A \square)$, phase $B(A \square)$, phase $Z(Z \square)$, CW pulse (CW $\square$ ), and CCW pulse (CCW $\square$ ). |
| Front connection section | Connectors CN1 and CN2 (Compatible connector: Sockets \& Hoods provided as standard accessories.) |
| Current consumption (Supplied from Power Supply Unit) | 5 V DC 160 mA max. |
| Dimensions | $25 \times 110 \times 107 \mathrm{~mm}(\mathrm{~W} \times \mathrm{H} \times \mathrm{D})$ |
| Weight | 90 g max. |
| Standard accessories | Sockets: XM2D-1501 (OMRON) x 2 <br> Hoods: XM2S-1511 (OMRON) x 2 |

## High-speed Counter Specifications

Counter Specifications

| Item |  |  | Specifications |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Number of counters |  |  | 2 counters (ports) |  |  |
| Input Modes (Set for each port in the PC Setup.) |  |  | Differential phase input | Pulse/Direction input | Up/Down pulse input |
| Input pin No. | Port 1 | Port 2 | --- |  |  |
|  | 3/10 | 3/10 | A-phase input | Direction input | Decrement pulse input |
|  | 4/11 | 4/11 | B-phase input | Pulse input | Increment pulse input |
|  | 2/9 | 2/9 | Z-phase input | Reset input | Reset input |
| Input method |  |  | Phase difference multiple of 4 (Fixed) | Single-phase pulse + direction | Single-phase pulse $\times 2$ |
| Count frequency |  |  | 25 KHz | 50 KHz | 50 KHz |
| Count value |  |  | Linear Mode: -8388608 to 8388607 <br> Ring Mode: 0 to 64999 (Maximum value can be set between 1 and 65000 with CTBL(63).) |  |  |
| Storage location of counter PV |  |  | Port 1: IR 233 (leftmost digits) and IR 232 (rightmost digits) <br> Port 2: IR 235 (leftmost digits) and IR 234 (rightmost digits) <br> Data format: 8-digit BCD <br> Linear Mode: F8388608 to 8388607 (Leftmost digit is F Hex for negative numbers.) <br> Ring Mode: 00000000 to 00064999 |  |  |
| Control method | Target value |  | Up to 48 target values and interrupt subroutine numbers registered. |  |  |
|  | Range comparison |  | Up to 8 upper limits, lower limits, and interrupt subroutine numbers registered. |  |  |
| Counter reset method |  |  | Phase-Z Signal + Softwa <br> A counter is reset on the fir turned ON. <br> Software Reset <br> A counter is reset when its <br> Reset Bits <br> Port 1: SR 25201 <br> Port 2: SR 25202 | Reset <br> phase-Z signal input <br> Reset Bit (see below) | s Reset Bit (see below) is $\mathrm{d} \mathrm{ON} .$ |

## Pulse Input Specifications

| Item | Specifications |  |  |
| :---: | :---: | :---: | :---: |
| Number of pulse inputs | 2 inputs (Ports 1 and 2 = Pulses 1 to 2) |  |  |
| Signal names | Encoder inputs A, encoder input B, pulse input Z |  |  |
| Input voltage | Switched by means of connector pins (Can be specified separately for phases A, B, and Z. |  |  |
|  | 12 V DC $\pm 10 \%$ | 24 V DC $\pm 10 \%$ |  |
| Input current | Phase A, B $\quad$ Phase Z | Phase A, B | Phase Z |
|  | 5 mA typical $\quad 12 \mathrm{~mA}$ typical | 5 mA typical | 12 mA typica |
| ON voltage | 10.2 V DC min. | 20.4 V DC min. |  |
| OFF voltage | 3.0 V DC min. | 4.0 V DC min. |  |
| Min. response pulse | Encoder inputs $A$ and $B$ <br> Waveform of encoder inputs $A$ and $B$ Input rise/fall time: $3 \mu \mathrm{sec}$. max. 50 kHz , pulse with duty factor of $50 \%$ <br> $3 \mu \mathrm{~s}$ max. $3 \mu \mathrm{~s}$ max. <br> Relationship between phases $A$ and $B$ when phase differential input is used. <br> Pulse input $Z$ <br> Pulse width must be 0.1 ms min. <br> T1, T2, T3, T4: $4.5 \mu \mathrm{~s}$ min. At least $4.5 \mu \mathrm{~s}$ must be allowed between Phase A and Phase B changes. |  |  |

## Pulse Output Specifications

## Pulse Output Functions

Pulse output functions are determined by the output method, as indicated below.

| Item | Specifications |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Fixed duty factor |  |  | Variable duty factor |
|  | Without trapezoidal acceleration/ deceleration | Same acceleration/ deceleration rates | Separate acceleration/ deceleration rates |  |
| Instruction | $\begin{aligned} & \hline \text { PULS(65)/ } \\ & \text { SPED(64) } \end{aligned}$ | PLS2(-) | $\begin{aligned} & \text { PULS(65)/ } \\ & \text { ACC(一) } \\ & \hline \end{aligned}$ | PWM(-) |
| Output frequency | 10 Hz to 50 kHz 10 Hz to 20 kHz for stepping motor | $\begin{aligned} & 0 \mathrm{~Hz} \text { to } \\ & 50 \mathrm{KHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{~Hz} \text { to } \\ & 50 \mathrm{KHz} \end{aligned}$ | $\begin{aligned} & 91.6 \mathrm{~Hz}, \\ & 1.5 \mathrm{KHz}, \\ & 5.9 \mathrm{KHz} \end{aligned}$ |
| Output frequency pitch | 1 or 10 Hz | 10 Hz |  | --- |
| Duty factor | 50\% fixed |  |  | 1 to 99\% |
| No. of output pulses | 1 to 16777215 |  |  | --- |
| Acceleration/ Deceleration rate | --- | 10 Hz to 2 kHz (every 4.08 ms ) |  | --- |


| Item | Specifications |
| :--- | :--- |
| No. of pulse outputs | 2 outputs (Ports 1 and 2 = Pulse outputs 1 and 2) |
| Signal names | CW and CCW pulse output |
| Max. output frequency | $50 \mathrm{kHz}(20 \mathrm{kHz}$ with stepping motor connected.) |
| External power supply | $5 \mathrm{~V} \mathrm{DC} \pm 5 \% 30 \mathrm{~mA}$ min. <br> $24 \mathrm{~V} \mathrm{DC}+10 \% /-15 \% 30 \mathrm{~mA} \mathrm{min}$. |
| Max. switching capacity | NPN open collector, $30 \mathrm{~mA} / 5 \mathrm{to} 24 \mathrm{~V} \mathrm{DC} \pm 10 \%$ |
| Min. switching capacity | NPN open collector, $7 \mathrm{~mA} / 5$ to $24 \mathrm{~V} \mathrm{DC} \pm 10 \%$ |
| Leakage current | 0.1 mA max. |
| Residual voltage | 0.4 V max. |
| Pulse output <br> specifications | Min. pulse width <br> ON tav |


| Pulse frequency | Switching current/Load power supply voltage |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | 7 to $30 \mathrm{~mA} / 5 \mathrm{~V}$ DC $\pm 10 \%$ |  | 7 to $30 \mathrm{~mA} / 24 \mathrm{~V}$ DC +10\%/-15\% |  |
|  | tON | tOFF | tON | tOFF |
| 10 kpps max. | $49.5 \mu \mathrm{~s}$ min. | $48.5 \mu \mathrm{~s}$ min. | $49.6 \mu \mathrm{~s}$ min. | $46.0 \mu \mathrm{~s}$ min. |
| 30 kpps max. | $19.5 \mu \mathrm{~s}$ min. | $18.5 \mu \mathrm{~s} \mathrm{~min}$. | $19.6 \mu \mathrm{~s}$ min. | $16.0 \mu \mathrm{~s} \mathrm{~min}$. |
| 50 kpps max. | $9.5 \mu \mathrm{~s} \mathrm{~min}$. | $8.5 \mu \mathrm{~s}$ min. | $9.6 \mu \mathrm{~s} \mathrm{~min}$. | $6.0 \mu \mathrm{~s} \mathrm{~min}$. |

## 8-3 Absolute Encoder Interface Board

## 8-3-1 Model

| Name | Model | Specifications |
| :--- | :--- | :--- |
| Absolute Encoder <br> Interface Board | CQM1H-ABB21 | 2 inputs for absolute encoders |

## 8-3-2 Functions

## Absolute High-speed Counter with Interrupt Function

The Absolute Encoder Interface Board is an Inner Board that counts two gray binary code inputs from an absolute (ABS) rotary encoder.

The Absolute Encoder Interface Board reads binary gray codes (inverted binary codes) input from an absolute encoder through ports 1 and 2 at a maximum counting rate of 4 kHz , and performs processing according to the input values.

## Operating Modes

BCD Mode and $360^{\circ}$ Mode.

## Resolutions

One of the following can be set: 8 bits ( 0 to 255), 10 bits ( 0 to 1023), or 12 bits ( 0 to 4095). The resolution should be set to match that of the encoder connected.

## Interrupts

An interrupt subroutine can be executed when the PV (present value) of the absolute high-speed counter matches a specified target value or lies within a specified comparison range.

Note The use of an absolute encoder means that the position data can be retained even during power interrupts, removing the need to perform an origin return when power is returned. In addition, the origin compensation function allows the user to specify any position as the origin.

Operation will be as illustrated below when the program is executed.


## 2-2 Pulse I/O Board

## 2-2-1 Model

| Name | Model | Specifications |
| :---: | :--- | :--- |
| Pulse I/O Board | CQM1H-PLB21 | Two pulse input points and two <br> pulse output points |

## 2-2-2 Function

Pulse Inputs 1 and 2

Pulse Outputs 1 and 2

Ports 1 and 2
The Pulse I/O Board is an Inner Board that supports two pulse inputs and two pulse outputs.

Pulse inputs 1 and 2 can be used as high-speed counters to count pulses input at either 50 kHz (signal phase) or 25 kHz (differential phase). Interrupt processing can be performed based on the present values (PV) of the counters.

## Input Mode

The following three Input Modes are available:

- Differential Phase Mode (4x)
- Pulse/Direction Mode
- Up/Down Mode


## Interrupts

The Board can be set to execute an interrupt subroutine when the value of the high-speed counter matches a specified target value, or an interrupt subroutine when the PV falls within a specified comparison range.

Two 10 Hz to 50 kHz pulses can be output from port 1 and port 2. Both fixed and variable duty factors can be used.

- The fixed duty factor can raise or lower the frequency of the output from 10 Hz to 50 kHz smoothly.
- The variable duty factor enables pulse output to be performed using a duty factor ranging from $1 \%$ to $99 \%$.
Note While pulse inputs and pulse outputs can be performed simultaneously, it is not possible to use all high-speed counter and pulse output functionality at the same time. The Port Mode Setting (High-speed Counter Mode/Simple Positioning Mode) in the PC Setup (DM 6611) will determines which has full functionality enabled.
Two pulse inputs (high-speed counter) and two pulse outputs can be used simultaneously via ports 1 and 2 . To determine which has functional priority, the appropriate Port Mode setting must be entered in the PC Setup (DM 6611).

| Mode | Content | High-speed counter functions |  | Pulse output functions |  |  | DM 6611 setting |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Reading PV with PRV(62) | Highspeed counter interrupts with CTBL(63) | No trapezoidal acceleration/ deceleration (SPED(64)) | $\begin{gathered} \text { Identical } \\ \text { acceleration/ } \\ \text { deceleration } \\ \text { rates } \\ \text { (PLS2(一)) } \end{gathered}$ | Separate acceleration/ deceleration rates $(\operatorname{ACC}(-))$ |  |
| Highspeed Counter Mode | High-speed counter given priority. <br> All high-speed counter functions are enabled. <br> Trapezoidal acceleration/ deceleration for pulse outputs is limited. | Yes | Yes | Yes |  | Mode 0 disabled (Modes 1 to 3 enabled) See note 1. | $\begin{aligned} & 0000 \\ & \mathrm{Hex} \end{aligned}$ |
| Simple Positioning Mode | Pulse output given priority. <br> All pulse output functions are enabled. <br> Interrupts for the high-speed counter are disabled. | Yes | No | Yes | Yes | Yes | $\begin{aligned} & 0001 \\ & \mathrm{Hex} \end{aligned}$ |

Note 1. Mode 0: Acceleration + Independent Mode; Mode 1: Acceleration + Continuous Mode; Mode 2: Deceleration + Independent Mode; Mode 3: Deceleration + Continuous Mode.
2. The port modes for both ports 1 and 2 is always set to the same mode, i.e., either High-speed Counter Mode and Simple Positioning Mode. The mode cannot be set separately for each port.

## 2-2-3 System Configuration



## 2-2-4 Applicable Inner Board Slot

The Pulse I/O Board can only be mounted in slot 2 (right slot) of the CQM1HCPU51/61 CPU Unit.


## 2-2-5 Names and Functions

The CQM1H-PLB21 Pulse I/O Board has a CN1 connector for pulse input 1 and pulse output 1, and a CN2 connector for pulse input 2 and pulse output 2.

## CQM1H-PLB21 Pulse I/O Board



Compatible connector
Socket: XM2D-1501 (OMRON)
Hood: XM2S-1511 (OMRON)
Two Sockets and two Hoods are provided as standard with the Pulse I/O Board.

## LED Indicators

Ready (green)
Lit when the pulse I/O functions are ready.


Lit when there is an error in the PC Setup settings for pulse I/O, or when operation is interrupted during pulse output.

## Pulse Output Indicators

| Indicator | Port | Function |
| :---: | :---: | :---: |
| CW1 | Port 1 | Lit during CW pulse output to port 1. |
| CCW1 |  | Lit during CCW pulse output to port 1. |
| CW2 | Port 2 | Lit during CW pulse output to port 2. |
| CCW2 |  | Lit during CCW pulse output to port 2. |

## Pulse Input Indicators

| Port 1 | Port 2 | Function |
| :--- | :--- | :--- |
| A1 | A2 | Lit when the phase-A pulse input is ON at the port. |
| B1 | B2 | Lit when the phase-B pulse input is ON at the port. |
| Z1 | Z2 | Lit when the phase-Z pulse input is ON at the port. |

## 2-2-6 Specifications

## High-speed Counter Specifications

## Instructions

| Instruction | Control | Meaning |
| :--- | :--- | :--- |
| (@)CTBL(63) | Range comparison table registration + <br> comparison start | Registers range comparison table and starts <br> comparison. |
|  | Target value table registration + comparison <br> start | Registers target value table and starts <br> comparison. |
|  | Range comparison table registration | Registers range comparison table. |
|  | Target value table registration | Registers target value table. |
|  | Comparison start | Starts comparison using registered <br> comparison table. |
|  | Comparison stop | Stops comparison. |
|  | PV change | Changes PV of high-speed counter. |
| (@)INT(89) | PV read | Reads PV of high-speed counter. |
|  | Status read | Reads status of high-speed counter. |
|  | Range comparison result read | Reads range comparison result. |
|  | Masking all interrupts | asking all interrupts, such as input interrupts, <br> interval limer interrupts, and high-speed <br> counter interrupts. |
|  | Clearing interrupt masks | Clears masks from interrupts. |
|  |  |  |

## Relevant Flags and

Control Bits for Pulse
Inputs
Bits for Slot 2 of Inner Board when Using Pulse I/O Board

| Word | Bits | Name |  | Function |
| :--- | :--- | :--- | :--- | :--- |
| IR 232 | 00 to 15 | Port 1 | PV word (rightmost four <br> digits) | The PV of the high-speed counter for each port of <br> the Pulse I/O Board is stored as an 8-digit BCD |
|  |  |  | PV word (leftmost four <br> digits) |  |
| value after each cycle. |  |  |  |  |

## SR Area Bits

| Word | Bit | Name | Function |
| :---: | :---: | :---: | :---: |
| SR 252 | 01 | High-speed Counter 1 Reset Bit (port 1) | Phase Z and software reset <br> 0 : Counter not reset on phase $Z$ <br> 1: Counter reset on phase $Z$ |
|  | 02 | High-speed Counter 2 Reset Bit (port 2) | Software reset only 0: Counter not reset $0 \rightarrow 1$ : Counter reset |

AR Area Flags

| Word | Bit | Name |  | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AR 05 | 00 | Port 1 | High-speed Counter 1 Range Comparison Flags | ON when meeting first condition. | When the high-speed counter is used for range comparisons, a flag turns ON when the corresponding condition is met. |
|  | 01 |  |  | ON when meeting second condition. |  |
|  | 02 |  |  | ON when meeting third condition. |  |
|  | 03 |  |  | ON when meeting fourth condition. |  |
|  | 04 |  |  | ON when meeting fifth condition. |  |
|  | 05 |  |  | ON when meeting sixth condition. |  |
|  | 06 |  |  | ON when meeting seventh condition. |  |
|  | 07 |  |  | ON when meeting eighth condition. |  |
|  | 08 |  | High-speed Counter 1 Comparison Flag | Indicates the status of th <br> 0: Stopped <br> 1: Running | comparison operation. |
|  | 09 |  | High-speed Counter 1 Overflow/Underflow Flag | Indicates the overflow/u <br> 0: Normal (No overflow/u <br> 1: Overflow/Underflow h | derflow status of the PV. nderflow) s occurred. |
| AR 06 | 00 | Port 2 | High-speed Counter 2 Range Comparison | ON when meeting first condition. | When the high-speed counter is used in range |
|  | 01 |  | Flags | ON when meeting second condition. | comparison format, a flag turns ON when the corresponding condition |
|  | 02 |  |  | ON when meeting third condition. | is met. |
|  | 03 |  |  | ON when meeting fourth condition. |  |
|  | 04 |  |  | ON when meeting fifth condition. |  |
|  | 05 |  |  | ON when meeting sixth condition. |  |
|  | 06 |  |  | ON when meeting seventh condition. |  |
|  | 07 |  |  | ON when meeting eighth condition. |  |
|  | 08 |  | High-speed Counter 2 Comparison Flag | Indicates the status of th <br> 0: Stopped <br> 1: Running | comparison operation. |
|  | 09 |  | High-speed Counter 2 Overflow/Underflow Flag | Indicates the overflow/un 0: Normal (No overflow/ <br> 1: Overflow/Underflow h | derflow status of the PV. nderflow) <br> as occurred. |

## SR Area Flags

| Word | Bit | Function |
| :---: | :--- | :--- |
| SR 254 | 15 | Inner Board Error Flag |

## AR Area Flags

| Word | Bit | Function |  |
| :--- | :--- | :--- | :--- |
| AR 04 | 08 to 15 | Error codes for Inner Board in slot 2 <br>  <br>  | 00 Hex: Normal <br> 01,02 Hex: Hardware error <br> 03 Hex: PC Setup error |

Relevant PC Setup Settings

| Word | Bits | Function |  | When activated |
| :---: | :---: | :---: | :---: | :---: |
| DM 6611 | 00 to 15 | Port Mode Setting (for ports 1 and 2) 0000 Hex: High-speed Counter Mode 0001 Hex: Simple Positioning Mode |  | When power is turned ON. |
| DM 6643 | 00 to 03 | Port 1 | High-speed counter input mode 0 Hex: Differential phase input <br> 1 Hex: Pulse/Direction input <br> 2 Hex: Up/Down pulse input | When operation starts. |
|  | 04 to 07 |  | High-speed counter reset method <br> 0 Hex: Phase-Z signal + software reset <br> 1 Hex: Software reset |  |
|  | 08 to 11 |  | High-speed counter numeric range 0 Hex: Linear Mode <br> 1 Hex: Ring Mode |  |
|  | 12 to 15 |  | (Setting for pulse output use.) |  |
| DM 6644 | 00 to 03 | Port 2 | High-speed counter input mode <br> 0 Hex: Differential phase input <br> 1 Hex: Pulse/Direction input <br> 2 Hex: Up/Down pulse input |  |
|  | 04 to 07 |  | High-speed counter reset method <br> 0 Hex: Phase-Z signal + software reset <br> 1 Hex: Software reset |  |
|  | 08 to 11 |  | High-speed counter numeric range <br> 0 Hex: Linear Mode <br> 1 Hex: Ring Mode |  |
|  | 12 to 15 |  | (Setting for pulse outputs.) |  |

## Pulse Output Specifications

Instructions
Pulse outputs are controlled using the seven instructions shown in the following table. The table also shows the relationship between the instruction and the type of pulse output.

| Instruction | Control summary | Single-phase pulse output without acceleration/ deceleration | Single-phase pulse output with same acceleration/ deceleration rates | Single-phase pulse output with separate acceleration/ deceleration rates | Variable duty factor pulse output |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PULS(65) (SET PULSES) | Sets number of output pulses. | Yes (Independent Mode only) | --- | Yes (Independent Mode only) | --- |
| SPED(64) <br> (SPEED OUTPUT) | Controls pulse outputs without acceleration/deceleration. | Yes | --- | --- | --- |
| PLS2(-) <br> (PULSE OUTPUT) | Controls trapezoidal acceleration/deceleration pulse outputs having same acceleration/deceleration rate. | --- | Yes | --- | --- |
| $\begin{aligned} & \text { ACC(-) } \\ & \text { (ACCELERATION } \\ & \text { CONTROL) } \end{aligned}$ | Controls trapezoidal acceleration/deceleration pulse outputs having separate acceleration/deceleration rate. | --- | --- | Yes | --- |
| PWM(—) <br> (PULSE WITH <br> VARIABLE DUTY <br> FACTOR) | Controls variable duty factor pulse outputs. | --- | --- | --- | Yes |
| $\begin{array}{\|l} \hline \text { INI(61) } \\ \text { (MODE } \\ \text { CONTROL) } \\ \hline \end{array}$ | Halts pulse output. | Yes | Yes | Yes | Yes |
| PRV(62) (HIGH-SPEED COUNTER PV READ) | Reads pulse output status. | Yes | Yes | Yes | Yes |

Instructions Applicable during Output
Some instructions relating to pulse output cannot be altered once output has begun. The following table lists those instructions that can and cannot be executed to change pulse output after another instruction has been executed (i.e., while pulse output is being performed as a result of a former instruction).

| Instruction that started pulse output | Instruction used to change pulse output |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | SPED <br> (Inde-pendent) | SPED (Continuous) | PULS <br> (0 or 1: Pulse setting) | PULS <br> (2 or 3: pulse acceleration/ deceleration setting) | PULS <br> (4 or 5: No pulse setting) | PLS2 | ACC <br> Mode 0 <br> (Acceleration <br> + Inde-pendent) | ACC Mode 1 (Acceleration + Con-tinuous) | ACC <br> Mode 2 <br> (Decel- <br> eration <br> + Inde-pendent) | ACC Mode 3 (Deceleration + Con-tinuous) | PWM |
| SPED(64) <br> (Independent Mode | Enabled | --- | --- | --- | --- | --- | Enabled | --- | Enabled | --- | --- |
| SPED(64) <br> (Continuous Mode) | Enabled | Enabled | Enabled | Enabled | --- | --- | --- | Enabled | --- | Enabled | --- |
| PULS(65) 0,1 <br> (Pulse setting) | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | --- | Enabled | Enabled | Enabled | --- |
| $\begin{aligned} & \text { PULS(65) 2,3 } \\ & \text { (Pulse } \\ & \text { acceleration/ } \\ & \text { deceleration } \\ & \text { setting) } \\ & \hline \end{aligned}$ | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | Enabled | --- |
| PULS(65) 3,4 <br> (No pulse setting) | --- | Enabled | Enabled | Enabled | Enabled | Enabled | --- | Enabled | --- | Enabled | --- |
| PLS2(-) | --- | --- | --- | --- | --- | --- | --- | --- | Enabled when stopped | --- | --- |
| ACC(-) <br> Mode 0 (Acceleration + Independent) | --- | --- | --- | --- | --- | --- | --- | --- | Enabled | --- | --- |
| ACC(-) <br> Mode 1 <br> (Acceleration $+$ Continuous) | --- | Enabled for constant speed | Enabled (see note) | Enabled (see note) | --- | --- | --- | Enabled for constant speed | --- | Enabled | --- |
| ACC(-) <br> Mode 2 <br> (Deceleration <br> Independent) | Enabled for constant speed | --- | --- | --- | --- | --- | --- | --- | Enabled | --- | --- |
| ACC(-) <br> Mode 0 <br> (Deceleration <br> $+$ <br> Continuous) | --- | Enabled for constant speed | Enabled (see note) | Enabled (see note) | Enabled (see note) | --- | --- | Enabled for constant speed | --- | Enabled | --- |
| PWM(-) | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | Enabled |

Note The number of pulses can be changed, but the direction cannot be changed.

Relevant Flags and
Control Bits (for Pulse
Output)
Bits for Slot 2 of Inner Board when Using Pulse I/O Board

| Word | Bits |  | Name | Function |
| :---: | :---: | :---: | :---: | :---: |
| IR 236 | 00 to 15 | Port 1 | PV word (rightmost four digits) | The PV of the pulse output associated with each port of the Pulse I/O Board is stored as an 8-digit BCD after each cycle. When pulse output is not used, these bits can be used as internal auxiliary bits. |
| IR 237 | 00 to 15 |  | PV word (leftmost four digits) |  |
| IR 238 | 00 to 15 | Port 2 | PV word (rightmost four digits) |  |
| IR 239 | 00 to 15 |  | PV word (leftmost four digits) |  |

AR Area Flags

| Word | Bit | Name  <br> Port 1 Deceleration Specified Flag <br> Pulse  <br> Output  <br> Flags  |  | Function |
| :---: | :---: | :---: | :---: | :---: |
| AR 05 | 12 |  |  | Indicates passage through deceleration point when deceleration is specified. <br> 0 : Not specified <br> 1: Specified |
|  | 13 |  | Number of Pulses Specified Flag | Indicates whether or not the number of pulses has been set using PULS(65). <br> 0 : Not specified <br> 1: Specified |
|  | 14 |  | Pulse Output Completed Flag | Indicates completion of the pulse output by SPED(64), PLS2(-), or ACC(一). <br> 0 : Not completed <br> 1: Completed |
|  | 15 |  | Pulse Output In Progress Flag | Indicates the execution status of the pulse output. <br> 0 : No pulse output <br> 1: Pulse output in progress |
| AR 06 | 12 | Port 2 <br> Pulse <br> Output <br> Flags | Deceleration Specified Flag | Indicates passage through deceleration point when deceleration is specified. <br> 0 : Not specified <br> 1: Specified |
|  | 13 |  | Number of Pulses Specified Flag | Indicates whether or not the number of pulses has been set using PULS(65). <br> 0: Not specified <br> 1: Specified |
|  | 14 |  | Pulse Output Completed Flag | Indicates completion of the pulse output by SPED(64), PLS2(-), or ACC(-). <br> 0 : Not completed <br> 1: Completed |
|  | 15 |  | Pulse Output In Progress Flag | Indicates the execution status of the pulse output. <br> 0 : No pulse output <br> 1: Pulse output in progress |

## Operation Timing Example



Note The status of the AR Area flags shown above may differ from the actual pulse output status due to the output frequency.

Relevant PC Setup Settings

| Word | Bit |  | Function | When setting is activated |
| :---: | :---: | :---: | :---: | :---: |
| DM 6611 | 00 to 15 | Port Mode Setting (ports 1 and 2) 0000 Hex: High-speed Counter Mode 0001 Hex: Simple Positioning Mode |  | When power is turned ON. |
| DM 6643 | 00 to 11 | Port 1 | (Setting for pulse input.) | When operation starts. |
|  | 12 to 15 |  | Fixed/Variable setting of pulse output duty factor 0 Hex: Use fixed duty factor pulse output (default). 1 Hex: Use variable duty factor pulse output. |  |
| DM 6644 | 00 to 11 | Port 2 | (Setting for pulse input.) |  |
|  | 12 to 15 |  | Fixed/Variable setting of pulse output duty factor 0 Hex: Use fixed duty factor pulse output (default). 1 Hex: Use variable duty factor pulse output. |  |

## 2-2-7 High-speed Counters 1 and 2

Pulse signals from rotary encoders to ports 1 and 2 of the Pulse I/O Board can be counted at high speed, and interrupt processing can be executed according to the number of pulses counted. The two ports can be used independently, and the counters used for ports 1 and 2 are high-speed counter 1 and high-speed counter 2.
This section describes how to use high-speed counters 1 and 2.
Note The instructions that can be used are limited by the port mode setting of the Board, which is set in the DM 6611 of the PC Setup.

Port Mode Setting and Applicable Instructions
In Simple Positioning Mode, CTBL(63) (REGISTER COMPARISON TABLE) cannot be used, and high-speed counter interrupts cannot be performed. Only PV reads can be performed.

| Instruction | CTBL(63) | INI(61) | PRV(62) |
| :--- | :--- | :--- | :--- |
| Function | Comparison table <br> registration <br> Comparison start | PV change <br> Comparison <br> start/stop | PV read <br> Comparison status <br> read <br> Range comparison <br> result read |
| High-speed <br> Counter Mode | Enabled | Enabled | Enabled |
| Simple Positioning <br> Mode | Disabled | Enabled (PV <br> change only) | Enabled |

## Processing

## Input Signals and Input Modes

The Input Modes that can be used for high-speed counters 1 and 2 are determined by the signal types.

1, 2, 3... 1. Differential Phase Mode (Counting Rate $=25 \mathrm{kHz}$ ):
Two phase-difference 4 x signals (phase $A$ and phase B) and a phase- $Z$ signal are used for inputs. The count is incremented or decremented according to differences in the two phase signals.
2. Pulse/Direction Mode (Counting Rate $=50 \mathrm{kHz}$ ):

Phase A is the direction signal and phase B is the count pulse. The counter increments when the phase-A signal is OFF and decrements when it is ON.
3. Up/Down Mode (Counting Rate $=50 \mathrm{kHz}$ ):

Phase $A$ is the decrementing signal and phase $B$ is the incrementing signal.

The counter decrements when an A-phase pulse is detected and increments when a phase-B pulse is detected.


## Numeric Ranges

The range of values counted by high-speed counters 1 and 2 are determined by the following two modes.

## 1, 2, 3... 1. Ring Mode

In Ring Mode, the maximum value of the counting range can be set with CTBL(63). The counter will go from the maximum count value to 0 when incrementing, and from 0 to the maximum count value when decrementing; there are no negative values. The maximum count value +1 (i.e., the ring value) is entered as the setting. Settings can range from 1 to 65,000 , making the counting range 0 to 64,999.
2. Linear Mode

The counting range in Linear Mode is fixed at $-8,388,608$ to $8,388,607$. If the count falls below the lower limit an underflow is generated, and if it exceeds the upper limit an overflow is generated. The PV will remain at 08388607 for overflows and F838 8608 for underflows, counting or comparison will be stopped (and the comparison table retained), and AR 0509 (port 1) or AR 0609 (port 2) will be turned ON.

Ring Mode


Linear Mode


One of the methods in the following section should be used to reset the counter when restarting the counting operation. The counter will be reset automatically when program execution is started or stopped.
Note The following signal transitions are handled as forward (incrementing) pulses: Phase-A leading edge $\rightarrow$ phase-B leading edge $\rightarrow$ phase-A trailing edge $\rightarrow$ phase-B trailing edge.
The following signal transitions are handled as reverse (decrementing) pulses: Phase-B leading edge $\rightarrow$ phase-A leading edge $\rightarrow$ phase-B trailing edge $\rightarrow$ phase-A trailing edge.
The following two methods can be used to determine the timing by which the PV of the counter is reset (i.e., set to 0):

- Phase-Z signal + software reset
- Software reset

Either the phase-Z signal + software reset or software reset alone may be used to reset the PV of the count. These resets operate in the same way as for high-

## Count Check Methods for High-speed Counter Interrupts

speed counter 0 (the built-in high-speed counter). Refer to page 31 for details.
The Reset Bits of high-speed counters 1 and 2 are as follows:
Reset Bit of high-speed counter 1: SR 25201
Reset Bit of high-speed counter 2: SR 25202
Note 1. Since the reset bits for high-speed counters 1 and 2 (SR 25201 and SR 25202) are refreshed during each cycle, a flag must be ON for a minimum of 1 full cycle to be read reliably.
2. Even after a reset, the comparison table registration status, comparison execution status, and range comparison results are retained unchanged. (If a comparison was being executed before the reset, it will continue.)

Just as for high-speed counter 0 , the following two count check methods can be used for high-speed counters 1 and 2:

- Target value method
- Range comparison method

Refer to page 31 for a description of each method.
For the target value method, up to 48 conditions can be registered in the comparison table. When the PV of the counter matches one of the 48 registered comparison values, the corresponding interrupt subroutine will be executed.
For the range comparison method, 8 comparison conditions are always registered in the comparison table. When the PV of the counter lies within the upper and lower limits for one of the ranges 1 to 8 , the corresponding interrupt subroutine will be executed.

## Procedure for Use



Input Modes:
Differential Phase, Pulse/Direction, or Up/Down
Reset methods: Phase Z + software reset or Software reset
Numeric Range: Ring Mode or Linear Mode

Check method:
High-speed Counter Mode:
Target value interrupts, range comparison interrupts
Simple Positioning Mode:
No interrupts (PV read; range comparison result read)

## Port Mode

Input Modes: Differential Phase, Pulse/Direction, Up/Down
Reset methods: Phase Z + software reset; Software reset
Numeric Range: Ring Mode; Linear Mode
REGISTER COMPARISON TABLE, CTBL(63):
Port-specific comparison table registration and comparison start
MODE CONTROL, INI(61):
Port-specific PV change and comparison start
HIGH-SPEED COUNTER PV READ, PRV(62):
Port-specific high-speed counter PV read, high-speed counter comparison status read, and range comparison result read
SUBROUTINE DEFINE, SBN(92) and RETURN, RET(93):
Creation of interrupt subroutines (Only when using high-speed counter 1 and 2 interrupts.)

Pulse I/O Board: High-speed Counter Function


Preliminary PC Setup
Before using high-speed counters 1 and/or 2, enter the following settings in PROGRAM mode.

## Port Mode Setting (DM 6611)

Specify High-speed Counter Mode for ports 1 and 2. This setting is read when the PC is turned ON . If it is changed, the PC must be restarted.


## Port Mode Setting

0000 Hex: High-speed Counter Mode
(Must be set to High-speed Counter Mode when using high-speed counter interrupts.)
0001 Hex: Simple Positioning Mode
Default: 0000 (High-speed Counter Mode)
Note 1. When using high-speed counter 1 and 2 interrupts, the port must be set to High-speed Counter Mode. Although the PV of the high-speed counter can be read in Simple Positioning Mode, high-speed counter 1 and 2 interrupts cannot be used.
2. This setting is only recognized when the CQM1H is started. To change the setting, turn the power OFF and then ON again before executing the program.
3. If DM 6611 is used to set ports 1 and 2 to Simple Positioning Mode, it is possible to use the $\operatorname{BCMP}(68)$ instruction to check the contents of the PV words of high-speed counters 1 and 2 (IR 232 to IR 235) and use this information in place of high-speed counter 1 and 2 interrupts. However, the PV obtained using this method may vary slightly from the actual PV.

## Port 1 and Port 2 Operation Settings

DM 6643 contains the settings for port 1, and DM 6644 contains the settings for port 2. These settings determine the operating parameters for these high-speed counters. Use settings that match the operating environment of each port.


Default: 0000 (Linear Mode, Z-phase and software reset, Differential Phase) Mode

## Input Refresh Word Settings

DM 6634 and DM 6635 contain the input refresh word settings for high-speed counters 1 and 2 respectively. Make these settings when it is necessary to refresh inputs before interrupt execution.

(Correspond to IR 000 to IR 015)
Default: 0000 (No input refresh)

## Programming

Use the following steps to program high-speed counters 1 and 2.
Note 1. High-speed counters 1 and 2 begin counting when the proper PC Setup settings are made.
2. The PVs of high-speed counters 1 and 2 are reset to 0 when power is turned ON, when operation begins, and when operation stops.
3. Comparison with the comparison table and interrupts will not be performed using the count operation alone.
4. The PV of high-speed counter 1 is stored in IR 232 and IR 233, and the PV of high-speed counter 2 is stored in IR 234 and IR 235.

## Starting and Stopping Comparison

1, 2, 3... 1. Use CTBL(63) to save the comparison table in the CQM1H and begin comparisons.


$$
\begin{aligned}
& \text { P: Port } \\
& \text { 001: Port } 1 \\
& \text { 002: Port } 2 \\
& \text { C: Mode } \\
& \text { 000: Target value table registered and comparison begun } \\
& \text { 001: Range table registered and comparison begun } \\
& \text { 002: Target table registered only } \\
& \text { 003: Range table registered only } \\
& \text { TB: Beginning word of comparison table }
\end{aligned}
$$

If C is set to 000 , then comparisons will be made using the target value method; if 001, they will be made using the range comparison method. In both cases the comparisons will begin after the comparison table is registered. While comparisons are being performed, high-speed counter 1 and 2 interrupts will be executed according to the comparison table. Refer to the explanation of CTBL(63) in Section 5 Instruction Set for details on the contents of the comparison tables that are saved.

Note Although setting the value of C to 002 registers a target value comparison table, and setting C to 003 registers a range comparison table, comparison does not start automatically. In these cases, $\mathrm{INI}(61)$ must be used to start the comparison operation.
2. To stop comparisons, execute $\operatorname{INI}(61)$ as shown below. Specify port 1 or 2 in $P(P=001$ or 002).


P: Port
001: Port 1
002: Port 2

Note 1. To restart comparisons, set the first operand to the port number, and the second operand to "000" (execute comparison), and execute the $\operatorname{INI}(61)$ instruction.
2. A table that has been registered will be retained in the CQM1H during operation (i.e., during program execution) until a new table is registered.

## Reading the PV of High-speed Counters 1 and 2

The following two methods can be used to read the PVs of high-speed counters 1 and 2:

- Reading the PV from memory
- Using PRV(62)


## Reading the PV from Memory

The PVs of high-speed counters 1 and 4 are stored in the corresponding data area words in the following way.

| Leftmost four digits | Rightmost four digits | Linear Mode | Ring Mode |  |
| :--- | :--- | :--- | :--- | :--- |
| Port 1: | IR 233 | IR 232 | F8388608 to 08388607 <br> $(-8,388,608$ to 8,388,607) | 00000000 to 00064999 |
| Port 2: | IR 235 | IR 234 | (The leftmost digit becomes F when the number is <br> negative.) |  |

Note These words are refreshed only once every cycle, so they may differ from the actual PV.

## Using PRV(62)

PRV(62) is used to read the PVs of high-speed counters 1 and 2. Specify highspeed counter 1 or 2 in $P(P=001$ or 002$)$.

$\begin{array}{cc}\text { P: Port } & \\ \text { 001: } & \text { Port } 1 \\ \text { 002: } & \text { Port } 2\end{array}$
D: First destination word
The PV of each high-speed counter is stored as shown below. In Linear Mode, the leftmost bit will be $F$ for negative values.

Leftmost four digits Rightmost four digits Linear Mode Ring Mode
$\mathrm{D}+1 \quad \mathrm{D} \quad \mathrm{F} 8388608$ to $08388607 \quad 00000000$ to 0006499

Note The PV can be read accurately at the time PRV(62) is executed.

## Changing the PV

There are two ways to change the PV of high-speed counters 1 and 2.

- Resetting to 0 using one of the reset methods
- Using $\mathrm{INI}(61)$

The method using $\operatorname{INI}(61)$ is explained here. Refer to Reset Methods on pagqeq5 for an explanation of the use of the reset methods.

## Changing the PV with INI(61)

Change the PV of high-speed counters 1 and 2 by using $\mathrm{INI}(61)$ as shown below.


| P: Port |  |
| :--- | :--- |
| 001: Port 1 |  |
| 002: Port 2 |  |
| P1: First PV word |  |

Leftmost four digits Rightmost four digits Linear Mode Ring Mode $\mathrm{P} 1+1 \quad \mathrm{P} 1 \quad \mathrm{~F} 8388608$ to 0838860700000000 to 0006499

To specify a negative number in Linear Mode, set F Hex in the leftmost digit.
Reading Status of High-speed Counters 1 and 2
There are 2 ways to read the status of high-speed counters 1 and 2:

- Reading the relevant flags in the AR area of the CQM1H
- Using PRV(62)


## Reading the Relevant AR Area Flags

The CQM1H data words relating to high-speed counters 1 and 2 are shown below. It is possible to know the status of high-speed counters 1 and 2 by reading these words.

## - Inner Board Error Codes

| Word | Bits | Function |  |  |
| :---: | :--- | :--- | :--- | :--- |
| AR 04 | 08 to 15 | Slot 2 | The stored error codes are as follows: |  |
|  |  |  | 00 Hex: | Normal |
|  |  |  | 01,02 Hex: | Hardware error |
|  |  |  | 03 Hex: | PC Setup error |

- Operating Status

| Word |  | Bit | Name | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Counter 1 | Counter 2 |  |  |  |  |
| AR 05 | AR 06 | 00 | High-speed Counter Range Comparison Flags | ON when meeting first condition. | When the high-speed counter is used in range comparison format, a bit turns ON when the corresponding condition is met. |
|  |  | 01 |  | ON when meeting second condition. |  |
|  |  | 02 |  | ON when meeting third condition. |  |
|  |  | 03 |  | ON when meeting fourth condition. |  |
|  |  | 04 |  | ON when meeting fifth condition. |  |
|  |  | 05 |  | ON when meeting sixth condition. |  |
|  |  | 06 |  | ON when meeting seventh condition. |  |
|  |  | 07 |  | ON when meeting eighth condition. |  |
|  |  | 08 | High-speed Counter Comparison Flag | Indicates the status of the comparison operation. <br> 0: Stopped <br> 1: Running |  |
|  |  | 09 | High-speed Counter Overflow/Underflow Flag | Indicates the overflow/underflow status of the PV. <br> 0: Normal (No overflow/underflow) <br> 1: Overflow/Underflow has occurred |  |

## Using PRV(62)

The status of high-speed counters 1 and 2 can also be determined by executing PRV(62). Specify high-speed counter 1 or 2 ( $\mathrm{P}=001$ or 002) and the destination word D. The status information will be written to bits 00 and 01 of D. Bits 02 to 15 will be set to 0 .


P: Port
001: Port 1
002: Port 2
D: Destination word
The status of the specified high-speed counter is stored in bits 00 and 01 of P1, as shown in the following table.

| Bit | Function |
| :--- | :--- |
| 00 | Comparison Operation Flag (0: Stopped; 1: Running) |
| 01 | High-speed Counter 1 and 2 PV Overflow/Underflow Flag (0: Normal; 1: <br> Underflow or overflow occurred) |

Bits 04 to 07 indicate the pulse output status; all other bits are 0 .
This example shows a program that outputs standard pulses from port 1 while counting those pulses with high-speed counter 1 . The high-speed counter operates in Up/Down Mode, with the pulse output's CW pulses incrementing the counter (B-phase input) and the CCW pulses decrementing the counter (Aphase input). Before executing the program, set the PC Setup as follows and restart the PC to enable the DM 6611 settings.
DM 6611: 0000 (High-speed Counter Mode).
DM 6643: 0002 (Port 1: Fixed duty factor pulse output, Linear Mode, Z-phase signal with software reset, and Up/Down Mode).
Other PC Setup settings use the default settings. (Inputs are not refreshed before interrupt processing.)

In addition, the following data is stored for the comparison table:
DM 0000: 0003 - Number of target values: 3
DM 0001: 2500 - Target value 1: 2,500
DM 0002: 0000
DM 0003: 0100 - Comparison 1 interrupt processing routine No.: 100
DM 0004: 7500 - Target value 2: 7,500
DM 0005: 0000
DM 0006: 0101 - Comparison 2 interrupt processing routine No.: 101
DM 0007: 0000 - Target value 3: 10,000
DM 0008: 0001
DM 0009: 0102 - Comparison 3 interrupt processing routine No.: 102


## 2－2－8 Functions

The pulse output functions of the Pulse I／O Board are given in the following table．

| Classification | Characteristics | Instructions used |
| :--- | :--- | :--- |
| Ports 1 and 2 pulse <br> output（Fixed duty <br> factor） | 10 Hz to $50(20) \mathrm{kHz}$ frequency． <br> Fixed duty factor． <br> Bidirectional output（CW and CCW）． <br> Frequency can be changed smoothly． | Set number of pulses：PULS（65） <br> Start pulse output：SPED（64） <br> Change frequency：SPED（64） <br> Stop pulse output：SPED（64）／INI（61） <br> Acceleration／Deceleration at same rate：PLS2（—） <br> Acceleration／Deceleration at separate rates：ACC（一） |
| Ports 1 and 2 pulse <br> output（Variable <br> duty factor） | $91.6 \mathrm{~Hz}, 1.5 \mathrm{kHz}$ ，or 5.9 kHz frequency． <br> Duty factor variable between $1 \%$ to $99 \%$. <br> Unidirectional output only． | Start pulse output：PWM（一） <br> Stop pulse output：INI（61） |

Note When a stepping motor is connected to the pulse output of port 1 or 2 ，use a max－ imum frequency not exceeding 20 kHz ．

## 2－2－9 Fixed Duty Factor Pulse Output

The following is a description of the procedure for performing pulse outputs from ports 1 and 2 using a duty factor of $50 \%$ ．
Outline
Pulse outputs from ports 1 and 2 are performed as shown in the diagram below． Ports 1 and 2 can be used simultaneously．The pulse output of each port can be switched to either CW（clockwise）or CCW（counterclockwise）direction．


When outputting pulses from ports 1 and 2，the frequency can be changed in steps or by a specified rate，as shown in the following diagram．


Pulse output from ports 1 and 2 can be performed in the following two modes：
－Continuous Mode：Pulse output continues until it is stopped by either a SPED（64）instruction or an $\mathrm{INI}(61)$ instruction．
－Independent Mode：Pulse output stops automatically when a specified num－ ber of pulses has been output．Output can also be stopped by a SPED（64）or $\mathrm{INI}(61)$ instruction．
Note Use INI（61）when pulse output has to be stopped immediately，as for an emer－ gency stop，etc．Pulse output will not stop even if a SPED（64），PLS2（一），or ACC（－）signal turns input OFF．

Only stop pulse output when it is actually being output. Confirm the status of pulse output using the Pulse Output In Progress Flag (AR0515/AR0615).

The following table shows the types of frequency changes that can be made with combinations of PULS(65), SPED(64), INI(61), PLS2(-), and ACC(-).


## Single-phase Fixed Duty Factor Pulse Outputs

The following flowchart shows the procedure for using PULS(65) and SPED(64) to perform single-phase fixed duty factor pulse outputs without acceleration or deceleration.


Single-phase Fixed Duty Factor Pulse Output without Acceleration/Deceleration


Trapezoidal Pulse Output With Same Acceleration/ Deceleration

The following flowchart shows the procedure for using PLS2(-) to perform trapezoidal pulse outputs with the same acceleration/deceleration rate.


Simple Positioning Mode
(PLS2(-) cannot be used in High-speed Counter Mode.)

Port 1 or port 2.

Output:
CW/CCW with/without $1.6 \mathrm{k} \Omega$ resistance.
Power supply for output: 5 V DC/24 V DC

Port mode setting (DM 6611):
Simple Positioning Mode (DM 6611 to 0001 Hex). See Note.
Operation settings for ports 1 and 2 (DM 6643/DM 6644):
Set to fixed duty factor ( 0000 Hex ).
(PLS2(-) cannot be used in High-speed Counter Mode.)

PULSE OUTPUT, PLS2(-):
Port-specific trapezoidal acceleration/deceleration pulse output control with same acceleration/deceleration rate.
MODE CONTROL, INI(61):
Stop pulse output to a specified port.
HIGH-SPEED COUNTER PV READ, PRV(62):
Read pulse output status of a specified port.

Trapezoidal Acceleration/Deceleration Pulse Outputs


Trapezoidal Pulse Output With Different Acceleration/Deceleration

The following flowchart shows the procedure for using PULS(65) and ACC(一) to perform trapezoidal pulse outputs with different acceleration/deceleration rates.


Simple Positioning Mode:
All functions of ACC (-) can be used.
High-speed Counter Mode:
Modes 1 to 3 of ACC(-) can be used; Mode 0 (Acceleration + Independent) is disabled.

Port 1 or port 2.

Output:
CW/CCW with/without $1.6 \mathrm{k} \Omega$ resistance.
Power supply for output: 5/24 V DC

Port Mode Setting (DM 6611):
Set to High-speed Counter Mode (0000 Hex) or Simple Positioning Mode (0001 Hex). See note.
Operation settings for ports 1 and 2 (DM 6643/DM 6644):
Set to fixed duty factor.
Note: ACC(-) Mode 0 (Acceleration + Independent) cannot be used in High-speed Counter Mode.

SET PULSES, PULS(65):
Set number of output pulses for each port.
ACCELERATION CONTROL, ACC(-):
Port-specific trapezoidal acceleration/deceleration pulse output control with different acceleration/deceleration rates.
MODE CONTROL, INI(61):
Stop pulse output to a specified port.
HIGH-SPEED COUNTER PV READ, PRV(62):
Read pulse output status of a specified port.

Trapezoidal Acceleration/Deceleration Pulse Outputs


PC Setup Settings

Port Mode Setting and Instructions

Before outputting pulses from port 1 or 2, switch the PC to PROGRAM mode and enter the following settings in the PC Setup.

## Port Mode Setting (DM 6611)



0000 Hex: High-speed Counter Mode 0001 Hex: Pulse Output Mode

Default: 0000 (High-speed Counter Mode)
The instructions that can be used are limited by the Port Mode setting for ports 1 and 2 of the Pulse I/O Board. The Port Mode is specified in the PC Setup (DM 6611).
The following tables show the port mode settings and the instructions that can be used with various pulse outputs.
Pulse Output without Trapezoidal Acceleration/Deceleration
All instructions can be used regardless of the port mode setting.

| Instruction | PULS(65) | SPED(64) | INI(61) | PRV(62) |
| :--- | :--- | :---: | :---: | :---: |
| Function | Sets number <br> of pulses | Sets frequency | Stops pulse <br> output | Reads pulse <br> output status |
|  | (Used in combination.) |  |  |  |
|  | Enabled |  |  |  |
|  | Enabled |  |  |  |

## Pulse Output with Trapezoidal Acceleration/Deceleration and the Same

 Acceleration/Deceleration RatePLS2(-) (PULSE OUTPUT) cannot be used in High-speed Counter Mode. It is not possible to perform trapezoidal acceleration/deceleration pulse output using the same acceleration/deceleration rates.

| Instruction | PLS2(一) | INI(61) | PRV(62) |
| :--- | :--- | :--- | :--- |
| Function | Sets number of <br> pulses | Stops pulse output | Reads pulse <br> output status |
| High-speed <br> Counter Mode | Disabled | Enabled |  |
| Simple Positioning <br> Mode | Enabled |  |  |

Pulse Output with Trapezoidal Acceleration/Deceleration and Separate Acceleration/Deceleration Rates
The only limitation that exists is that ACC(一) (ACCELERATION CONTROL) in Mode 0 (Acceleration + Independent) cannot be used in High-speed Counter Mode.

| Instruction | PULS(65) | ACC(一) | INI(61) | PRV(62) |
| :---: | :--- | :--- | :--- | :---: |
| Function | Sets number <br> of pulses | Acceleration/ <br> Deceleration <br> rates <br> (separate <br> settings) <br> Sets frequency <br> Starts pulse <br> output | Stops pulse <br> output | Reads pulse <br> output status |
| High-speed <br> Counter Mode | Enabled | Mode 0 (Acc.+ <br> Independent): <br> Disabled <br> Mode 3: <br> Enabled | Enabled |  |
|  | Used in combination.) |  |  |  |
| Simple <br> Positioning <br> Mode | Enabled |  |  |  |

The setting in DM 6611 is read only when the CQM1H is started. If this setting is changed, the PC must be turned OFF and ON again to enable the new value.

## Operation Settings for Ports 1 and 2 (DM 6643 and DM 6644)

The diagram below shows how port 1 (DM 6643) and port 2 (DM 6644) are set to perform fixed duty factor pulse output, which is the default pulse output format. The settings for ports 1 and 2 can differ.


Variable duty factor pulses cannot be output from a port if it has been set to perform standard pulse output.

The following examples show programs that controls pulse output from ports 1 and 2. Before running the programs, check that the settings in the PC Setup are as follows:
DM 6611: 0001 (Simple Positioning Mode)
DM 6643: 0000 (Fixed duty factor pulse output from port 1)
DM 6644: 0000 (Fixed duty factor pulse output from port 2)

## Starting Pulse Output at Specified Frequency

The following example shows PULS(65) and SPED(64) used to control a pulse output from port 1. The number of pulses specified in PULS(65) $(10,000)$ are out-
put as the frequency is changed by executions of SPED(64) with different frequency settings.


The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.

! Caution Be sure that the pulse frequency is within the motor's self-starting frequency range when starting and stopping the motor.

Note Speed control timing will be accurate when frequency changes are performed as input interrupt processes.

Example 2: Stopping Pulse Output with SPED(64)

The following example shows PULS(65) and SPED(64) used to control a pulse output from port 1. The frequency is changed by executions of $\operatorname{SPED}(64)$ with different frequency settings and finally stopped with a frequency setting of 0 .


The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.


Be sure that the pulse frequency is within the motor's self-starting frequency range when starting and stopping the motor.

Example 3: Using
PLS2(-) to Accelerate/ Decelerate the Frequency at the Same Rate

The following example shows PLS2(-) used to output 100,000 CW pulses from port 1. The frequency is accelerated to 10 kHz at approximately $500 \mathrm{~Hz} / 4 \mathrm{~ms}$ and decelerated at the same rate.

Five seconds after the CW pulses have been output, another PLS2(-) instruction outputs 100,000 CCW pulses with the same settings.

| DM 0000 | 0050 |
| :--- | :--- |
| DM 0001 | 1000 |
| DM 0002 | 0000 |
| DM 0003 | 0010 |



The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.


Example 4: Using
ACC(一) to Accelerate/ Decelerate the Frequency at Different Rates

Example 5: Using
ACC(-) to Accelerate the Frequency at a Specified Rate

The following example shows Mode 0 of ACC(-) used to output 10,000 CW pulses from port 1. The frequency is accelerated to 10 kHz at approximately $1 \mathrm{kHz} / 4 \mathrm{~ms}$ and decelerated to 1 kHz at approximately $250 \mathrm{~Hz} / 4 \mathrm{~ms}$. Deceleration begins after 9,100 pulses have been output.

| DM 0000 | 0000 |
| :--- | :--- |
| DM 0001 | 0001 |
| DM 0002 | 9100 |
| DM 0003 | 0000 |


| DM 0004 | 0100 |
| :---: | :---: |
| DM 0005 | 1000 |
| DM 0006 | 0025 |
| DM 0007 | 0050 |



When IR 00000 turns ON, PULS(65) sets port 1 for CW pulse output. The total number of pulses is set to 10,000 and the deceleration point is set to 9,100 pulses.

Starts CW pulse output from port 1.
Acceleration rate: Approx. $1000 \mathrm{~Hz} / 4 \mathrm{~ms}$
Target frequency after acceleration: $10,000 \mathrm{~Hz}$
Deceleration rate: Approx. $250 \mathrm{~Hz} / 4 \mathrm{~ms}$
Target frequency after deceleration: 1 kHz
Following deceleration, pulse output starts at target frequency of approx. $500 \mathrm{~Hz} / 4 \mathrm{~ms}$.

The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.


The following example shows Mode 1 of $\operatorname{ACC}(-)$ used to increase the frequency of a pulse output from port 1. The frequency is accelerated from 1 kHz to 20 kHz at approximately $500 \mathrm{~Hz} / 4 \mathrm{~ms}$.

| DM 0000 | 0050 |
| :--- | :--- |
| DM 0001 | 2000 |

Example 6: Using
ACC(-) to Decelerate the Frequency at a Specified Rate and Stop Output

## Example 7: Using

ACC(-) to Decelerate the Frequency at a Specified Rate

The following diagram shows the frequency of pulse outputs from port 2 as the program is executed.


The following example shows Mode 2 of $\mathrm{ACC}(-)$ used decrease the frequency of a pulse output from port 1 . The $2-\mathrm{kHz}$ pulse output is already in progress in independent mode and stops automatically when the number of pulses is reached.

| DM 0000 | 0050 |
| :--- | :--- |
| DM 0001 | 0001 |



When IR 00000 turns ON, ACC(-) begins decelerating the port 1 pulse frequency at about $500 \mathrm{~Hz} / 4 \mathrm{~ms}$ until it reaches the target frequency of 10 Hz . Pulse output stops when the specified number of pulses is reached.

The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.


Note The pulse output can be stopped by executing ACC(-) Mode 2 with a target frequency of 0 . However, since the pulse output cannot be stopped at the correct number of pulses, this method should not be used except for emergency stops.

The following example shows Mode 3 of ACC(-) used to decrease the frequency of a pulse output from port 1 . The $20-\mathrm{kHz}$ pulse output is already in progress in Continuous Mode.

| DM 0000 | 0100 |
| :---: | :---: |
| DM 0001 | 0500 | port 1 pulse output at about $1,000 \mathrm{~Hz} / 4 \mathrm{~ms}$ until it reaches the target frequency of $5,000 \mathrm{~Hz}$.

The following diagram shows the frequency of pulse outputs from port 1 as the program is executed.


## 2-2-10 Variable Duty Factor Pulse Outputs

The following is the procedure for outputting pulses with varying duty factors (i.e., the ratio of the pulse ON time and the pulse cycle) from ports 1 and/or 2. This function can be used for various kinds of control outputs, such as light intensity output or speed control output to an inverter.

Outline
Variable duty factor pulse outputs from ports 1 and/or 2 are executed as shown in the diagram below. Ports 1 and 2 can be used at the same time.


## Variable Duty Factor Pulse Outputs Using PWM(一)



Port 1 or port 2.

Output:
PWM(-) with/without $1.6 \mathrm{k} \Omega$ resistance.
Power supply for output: 5/24 V DC

Port Mode Setting (DM 6611):
High-speed Counter Mode ( 0000 Hex ) or Simple Positioning Mode ( 0001 Hex )
Operation settings for ports 1 and 2 (DM 6643/DM 6644):
Set to variable duty factor ( 1000 Hex ).
PULSE WITH VARIABLE DUTY FACTOR, PWM(一):
Set frequency and duty factor.
MODE CONTROL, INI(61):
Stop pulse output to a specified port.
HIGH-SPEED COUNTER PV READ, PRV(62):
Read pulse output status of a specified port.

Variable Duty Factor Pulse Outputs


## PC Setup Settings

Before outputting variable duty factor pulses from port 1 or 2, switch the PC to PROGRAM Mode and make the following settings in the PC Setup.
Operation Settings of Ports 1 and 2
Make the following settings to set port 1 (DM 6643) or port 2 (DM 6644) to variable duty factor pulse output mode. Ports 1 and 2 can be set separately.


Note 1. When a port is set to variable duty factor pulse output, it cannot output fixed duty factor pulses.
2. When using variable duty factor pulse output, all instructions can be used, regardless of the Port Mode.

| Instruction | PWM(一) | INI(61) | PRV(62) |
| :--- | :--- | :--- | :--- |
| Function | Frequency setting <br> Duty factor setting <br> Pulse output start | Pulse output stop | Pulse output status <br> read |
| High-speed <br> Counter Mode | Enabled |  |  |
| Simple Positioning <br> Mode | Enabled |  |  |

## Starting the Pulse Output

PWM(一) is used to specify the port number, the pulse frequency, and the duty factor, and to start pulse output.


D: Duty factor
Specify either a 4-digit BCD constant or a word address where the value of $D$ is stored as a 4 -digit $B C D$ representing a percentage value. The setting must be between 0001 and 0099 (i.e., $1 \%$ to $99 \%$ ).

Pulse output will start using the settings specified by PWM(-), and will continue with those settings until PWM(-) is executed again with different settings, or until $\operatorname{INI}(61)$ is executed to stop pulse outputs from the specified port.

## Stopping the Pulse Output

The pulse output from a port can be stopped by executing $\operatorname{INI}(61)$ with $\mathrm{C}=003$. Specify port 1 or 2 ( $\mathrm{P}=001$ or 002).

| $@\|N\|(61)$ |
| :---: |
| $P$ |
| 003 |
| 000 |


| P: Port |  |
| :--- | :--- |
| 001: | Port 1 |
| 002: | Port 2 |

The following example shows PWM(一) used to start a 1.5 kHz pulse output from port 1 and then change the duty factor from $50 \%$ to $25 \%$. The pulse output is then stopped with $\mathrm{INI}(61)$. Before running the program, check that the settings in the PC Setup are as follows:

DM 6643: 1000 (variable duty factor pulse setting for port 1).


The following diagram shows the duty factor of the pulse output from port 1 as the program is executed.


## 2-2-11 Determining the Status of Ports 1 and 2

The status of pulse outputs (fixed or variable duty factor pulses) of ports 1 and 2 can be determined either by reading the status of the relevant flags in the SR and AR areas or by executing PRV(62).
Reading Flag Status
The memory words associated with the status of pulse outputs from ports 1 and 2 are shown in the following tables. The pulse output status can be determined by reading the contents of the words and flags shown in these words.

## - Inner Board Error Codes

| Word | Bits | Slot |  | Function |
| :--- | :--- | :--- | :--- | :--- |
| AR 04 | 08 to 15 | Slot 2 | Error codes are | stored as two-digit hexadecimals: |
|  |  |  | 00 Hex: | Normal |
|  |  |  | 01 and 02 Hex: | Hardware error |
|  |  |  | 02 Hex: | PC Setup error |
|  |  |  | 03 Hex: | PC stopped during |
|  |  |  |  | pulse output |

## - Operation Status Indicators

| Word |  | Bit | Name | Function |
| :---: | :---: | :---: | :---: | :---: |
| Port 1 | Port 2 |  |  |  |
| AR 05 | AR 06 | 12 | Deceleration Flag | Indicates the passage through a deceleration point when deceleration is specified. <br> 0 : Not specified <br> 1: Specified |
|  |  | 13 | Number of Pulses Flag | Stores whether or not the number of pulses have been specified. <br> 0 : Not specified <br> 1: Specified |
|  |  | 14 | Pulse Output Completed Flag | Indicates the completion status of the pulse output. <br> 0: Not completed <br> 1: Completed |
|  |  | 15 | Pulse Output Status Flag | Indicates the operation status of the pulse output. <br> 0 : Pulse output stopped <br> 1: Pulse output in progress |

## Using PRV(62)

The status of pulse outputs can be determined by using PRV(62). Specify port 1 or $2(\mathrm{P}=001$ to 002$)$ and the destination word D .


The bits comprising the pulse output status information stored in $D$ have the following meanings:

| Bit | Function | Description |
| :--- | :--- | :--- |
| 04 | Deceleration Flag | Indicates deceleration. <br> (0: Not decelerating; 1: Decelerating) |
| 05 | Number of Pulses <br> Flag | Indicates whether the total number of pulses have <br> been specified. (0: Not specified; 1: Specified.) |
| 06 | Pulse Output Com- <br> pleted Flag | Indicates whether pulse output has been completed. <br> (0: Not completed; 1: Completed.) |
| 07 | Pulse Output Status <br> Flag | Indicates whether pulses are being output. <br> (0: No output; 1: Output in progress.) |

In addition to the above, bits 0 and 1 store information about the status of the high-speed counter. All other bits are 0 .

Note When $\operatorname{PRV}(62)$ is used to read a port's status, the most recent information will be read regardless of the PC's cycle time.

## 2-2-12 Precautions When Using Pulse Output Functions

The Pulse I/O Board divides the 500 kHz source clock by an integer value to generate an output pulse frequency. For this reason, the frequency setting and the frequency actually produced may differ. Refer to the following formula to calculate the actual frequency.
Pulse Output Structure Setting frequency:
Output frequency set by User.
Division ratio:
An integer value set at the division circuit to generate output pulses of the set frequency.
Actual frequency:
Actual output pulse frequency produced by the division circuit.


INT: Function to derive integer value INT (500 / Set frequency): Division ratio

The difference between the set frequency and the actual frequency increases as the frequency increases, as shown in the examples in the following table.

| Set frequency (kHz) | Actual frequency $\mathbf{( k H z )}$ |
| :--- | :--- |
| 45.46 to 50.00 | 50.00 |
| 41.67 to 45.45 | 45.45 |
| 38.47 to 41.66 | 41.67 |
| 31.26 to 33.33 | 33.33 |
| 29.42 to 31.25 | 31.25 |
| 27.78 to 29.41 | 29.41 |
| 20.01 to 20.83 | 20.83 |
| 19.24 to 20.00 | 20.00 |
| 18.52 to 19.23 | 19.23 |
| 10.01 to 10.20 | 10.20 |
| 9.81 to 10.00 | 10.00 |
| 9.62 to 9.80 | 9.80 |
| 5.01 to 5.05 | 5.05 |
| 4.96 to 5.00 | 5.00 |
| 4.90 to 4.95 | 4.95 |
| 3.02 to 3.03 | 3.03 |
| 3.00 to 3.01 | 3.01 |
| 2.98 to 2.99 | 2.99 |

## 2-3 Absolute Encoder Interface Board

## 2-3-1 Model

| Name | Model | Specifications |
| :---: | :---: | :---: |
| Absolute Encoder <br> Interface Board | CQM1H-ABB21 | 2 inputs for absolute encoders |

